

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1-155*. (Canceled)

156. (New) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices on the principal surface; and

forming a stress-controlled dielectric membrane overlying the circuit devices.

157. (New) The method of claim 156, wherein the stress-controlled dielectric membrane comprises at least one stress-controlled dielectric layer.

158. (New) The method of claim 157, wherein the at least one stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less.

159. (New) The method of claim 158, wherein said stress is tensile.

* On May 29, 2003, a Notice of Allowance and Fee(s) Due was issued allowing claims 84-155 in parent Application No. 09/775,597.

160. (New) The method of claim 157, comprising forming the at least one stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

161. (New) The method of claim 160, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

162. (New) The method of claim 156, wherein the stress-controlled dielectric membrane is caused to have a stress of about 8×10^8 dynes/cm² or less.

163. (New) The method of claim 162, wherein said stress is tensile.

164. (New) The method of claim 156, wherein said substrate is a semiconductor wafer.

165. (New) The method of claim 156, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

166. (New) The method of claim 165, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

167. (New) The method of claim 156, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

168. (New) The method of claim 167, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

169. (New) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices on the principal surface; and

forming a stress-controlled dielectric layer overlying the circuit devices.

170. (New) The method of claim 169, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less.

171. (New) The method of claim 170, wherein said stress is tensile.

172. (New) The method of claim 169, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

173. (New) The method of claim 172, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

174. (New) The method of claim 169, wherein said substrate is a semiconductor wafer.

175. (New) The method of claim 169, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

176. (New) The method of claim 175, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

177. (New) The method of claim 169, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

178. (New) The method of claim 177, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

179. (New) A method of making an integrated circuit comprising:

providing a substrate having a principal surface; and

forming circuitry on the principal surface of the substrate with a stress-controlled dielectric layer.

180. (New) The method of claim 179, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less.

181. (New) The method of claim 180, wherein said stress is tensile.

182. (New) The method of claim 179, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

183. (New) The method of claim 182, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

184. (New) The method of claim 179, wherein said substrate is a semiconductor wafer.

185. (New) The method of claim 179, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

186. (New) The method of claim 185, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

187. (New) The method of claim 24, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

188. (New) The method of claim 187, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

189. (New) A method of using an integrated circuit having a stress-controlled dielectric layer and interconnections formed passing through the stress-controlled dielectric layer, the method comprising:
transferring information through the interconnections formed passing through the stress-controlled dielectric layer.

190. (New) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less.

191. (New) The method of claim 190, wherein said stress is tensile.

192. (New) The method of claim 189, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

193. (New) The method of claim 192, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

194. (New) The method of claim 189, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

195. (New) The method of claim 194, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

196. (New) The method of claim 189, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

197. (New) The method of claim 196, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

198. (New) A method of using an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, interconnect circuitry interconnecting the data source and the data sink, the interconnections formed within one or more stress-controlled dielectric layers, the method comprising:

transferring a plurality of data bytes between the data source and data sink of the interconnect circuitry of the integrated circuit.

199. (New) The method of claim 198, wherein the one or more stress-controlled dielectric layers are caused to have a stress of about 8×10^8 dynes/cm² or less.

200. (New) The method of claim 199, wherein said stress is tensile.

201. (New) The method of claim 198, further comprising forming the one or more stress-controlled dielectric layers by deposition of one or more stress-controlled dielectric films.

202. (New) The method of claim 201, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

203. (New) The method of claim 198, wherein the integrated circuit is able to have a major portion of the

substrate removed throughout a full extent thereof while retaining its structural integrity.

204. (New) The method of claim 203, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

205. (New) The method of claim 198, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

206. (New) The method of claim 205, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

207. (New) The method of claim 156, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

208. (New) The method of claim 156, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

209. (New) The method of claim 179, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

210. (New) The method of claim 179, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

211. (New) The method of claim 189, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

212. (New) The method of claim 189, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

213. (New) The method of claim 198, further comprising:

a second integrated circuit overlying the integrated circuit; and

interconnect connecting portions of the circuitry of the second integrated circuit and the integrated circuit.

214. (New) The method of claim 198, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

215. (New) The method of claim 157, wherein the at least one stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

216. (New) The method of claim 169, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

217. (New) The method of claim 179, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

218. (New) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

219. (New) The method of claim 120, wherein the one or more stress-controlled dielectric layers are caused to have a stress of about 8×10^8 dynes/cm² or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

220. (New) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices; and

forming a stress-controlled dielectric membrane overlying said active devices;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

221. (New) The method of claim 220, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

222. (New) The method of claim 220, wherein said substrate is a semiconductor wafer.

223. (New) The method of claim 220, further comprising removing a major portion of the substrate.

224. (New) The method of claim 223, wherein the major portion of the substrate is removed prior to forming said circuitry.

225. (New) The method of claim 223, wherein the major portion of the substrate is removed after forming said circuitry.

226. (New) The method of claim 220, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

227. (New) The method of claim 220, wherein the stress-controlled dielectric membrane is caused to have a stress of about 8×10^8 dynes/cm² or less.

228. (New) The method of claim 227, wherein said stress is tensile.

229. (New) The method of claim 220, wherein the stress-controlled dielectric membrane comprises at least one or more stress-controlled dielectric layers.

230. (New) The method of claim 220, wherein the major portion of the substrate is removed prior to forming said circuitry.

231. (New) The method of claim 220, wherein the major portion of the substrate is removed after forming said circuitry.

232. (New) The method of claim 220, comprising forming the stress-controlled dielectric membrane by deposition of one or more stress-controlled dielectric films.

233. (New) The method of claim 232, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

234. (New) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices; and

forming a stress-controlled dielectric layer overlying said active devices;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

235. (New) The method of claim 234, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

236. (New) The method of claim 234, comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

237. (New) The method of claim 236, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

238. (New) The method of claim 234, wherein said substrate is a semiconductor wafer.

239. (New) The method of claim 234, further comprising removing a major portion of the substrate.

240. (New) The method of claim 239, wherein the major portion of the substrate is removed prior to forming said circuitry.

241. (New) The method of claim 239, wherein the major portion of the substrate is removed after forming said circuitry.

242. (New) The method of claim 234, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

243. (New) The method of claim 234, wherein the stress-controlled dielectric membrane is caused to have a stress of about 8×10^8 dynes/cm² or less.

244. (New) The method of claim 243, wherein said stress is tensile.

245. (New) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices;

forming a stress-controlled dielectric layer overlying said active devices; and

removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

246. (New) The method of claim 245, wherein the major portion of the substrate is removed prior to forming said circuitry.

247. (New) The method of claim 245, wherein the major portion of the substrate is removed after forming said circuitry.

248. (New) The method of claim 245, comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

249. (New) The method of claim 248, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

250. (New) The method of claim 245, wherein said substrate is a semiconductor wafer.

251. (New) The method of claim 245, wherein the major portion of the substrate is removed prior to forming said circuitry.

252. (New) The method of claim 245, wherein the major portion of the substrate is removed after forming said circuitry.

253. (New) The method of claim 245, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

254. (New) The method of claim 245, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less.

255. (New) The method of claim 254, wherein said stress is tensile.

256. (New) The method of claim 220, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

257. (New) The method of claim 220, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

258. (New) The method of claim 234, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

259. (New) The method of claim 234, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

260. (New) The method of claim 245, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

261. (New) The method of claim 245, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

262. (New) The method of claim 229, wherein the at least one stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

263. (New) The method of claim 234, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

264. (New) The method of claim 245, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm² or less and the integrated circuit is caused to have a thickness of about 50 microns or less.